IN THE CLAIMS

Claims 48-49 are added; as a result, claims 23-49 are now pending in this application.

1-22. (Canceled)

23. (Previously Presented) A method of forming an integrated circuit, comprising:

forming an array of memory cells on a substrate;

coupling a substrate voltage level controller circuit to the substrate for setting a substrate voltage bias level including:

coupling a series of diodes between a supply voltage source and the substrate; and

coupling at least one bypass transistor to at least one diode in the series of diodes for electrically bypassing at least one diode, wherein the at least one bypass transistor is adapted for selective actuation to both an on state and an off state by a user while setting a substrate voltage bias level.

24. (Previously Presented) The method of claim 23 wherein coupling at least one bypass transistor to at least one diode includes coupling a plurality of bypass transistors to a plurality of diodes in the series of diodes for electrically bypassing the plurality of diodes.

25. (Previously Presented) The method of claim 23 wherein coupling at least one bypass transistor to at least one diode includes coupling at least one bypass transistor to plurality of diodes for electrically bypassing the plurality of diodes.

26. (Previously Presented) The method of claim 23 wherein coupling at least one bypass transistor to at least one diode includes coupling at least one normally off bypass transistor to at least one diode leaving the at least one diode unbypassed during normal operation and allowing the at least one diode to be selectively bypassed during testing operations.

27. (Previously Presented) The method of claim 23 wherein coupling at least one bypass transistor to at least one diode includes coupling at least one normally on bypass transistor to at least one diode leaving the at least one diode bypassed during normal operation and allowing the at least one diode to be selectively unbypassed during testing operations.

28. (Previously Presented) A method of forming an integrated circuit, comprising:

forming an array of memory cells on a substrate;

coupling a substrate voltage level controller circuit to the substrate for setting a substrate voltage bias level including:

coupling a series of diodes between a supply voltage source and the substrate; and

coupling at least one bypass transistor to a plurality of diodes in the series of diodes for electrically bypassing the plurality of diodes, wherein the at least one bypass transistor is adapted for selective actuation to both an on state and an off state by a user while setting a substrate voltage bias level.

29. (Previously Presented) The method of claim 28 wherein coupling at least one bypass transistor to a plurality of diodes includes coupling at least one normally off bypass transistor to a plurality of diodes leaving the plurality of diodes unbypassed during normal operation and allowing the plurality of diodes to be selectively bypassed during testing operations.

30. (Previously Presented) The method of claim 28 wherein coupling at least one bypass transistor to a plurality of diodes includes coupling at least one normally on bypass transistor to a plurality of diodes leaving the plurality of diodes bypassed during normal operation and allowing the plurality of diodes to be selectively unbypassed during testing operations.

31. (Previously Presented) A method of forming an integrated circuit, comprising:

forming an array of memory cells on a substrate;

coupling a substrate voltage level controller circuit to the substrate for setting a substrate

voltage bias level including:

coupling a series of diodes between a supply voltage source and the substrate; and

coupling a plurality of bypass transistors to a plurality of diodes in the series of diodes for electrically bypassing the plurality of diodes, wherein the at least one bypass transistor is adapted for selective actuation to both an on state and an off state by a user while setting a substrate voltage bias level.

32. (Previously Presented) The method of claim 31 wherein coupling a plurality of bypass transistors to a plurality of diodes includes coupling a plurality of normally off bypass transistors to a plurality of diodes leaving the plurality of diodes unbypassed during normal operation and allowing the plurality of diodes to be selectively bypassed during testing operations.

33. (Previously Presented) The method of claim 31 wherein coupling a plurality of bypass transistors to a plurality of diodes includes coupling a plurality of normally on bypass transistors to a plurality of diodes leaving the plurality of diodes bypassed during normal operation and allowing the plurality of diodes to be selectively unbypassed during testing operations.

34. (Previously Presented) A method of forming an integrated circuit, comprising:

forming an array of memory cells on a substrate;

coupling a substrate voltage level controller circuit to the substrate for setting a substrate voltage bias level including:

coupling a series of diode connected transistors between a supply voltage source and the substrate; and

coupling at least one bypass transistor to at least one diode connected transistor in the series of diode connected transistors for electrically bypassing at least one diode connected transistor, wherein the at least one bypass transistor is adapted for selective actuation to both an on state and an off state by a user while setting a substrate voltage bias level.

35. (Previously Presented) The method of claim 34 wherein coupling at least one bypass transistor to at least one diode connected transistor includes coupling at least one bypass transistor to plurality of diode connected transistors for electrically bypassing the plurality of diode connected transistors.

36. (Previously Presented) The method of claim 34 wherein coupling at least one bypass transistor to at least one diode connected transistor includes coupling at least one normally off bypass transistor to at least one diode connected transistor leaving the at least one diode connected transistor unbypassed during normal operation and allowing the at least one diode connected transistor to be selectively bypassed during testing operations.

37. (Previously Presented) The method of claim 34 wherein coupling at least one bypass transistor to at least one diode connected transistor includes coupling at least one normally on bypass transistor to at least one diode connected transistor leaving the at least one diode connected transistor bypassed during normal operation and allowing the at least one diode connected transistor to be selectively unbypassed during testing operations.

38. (Previously Presented) A method of forming an integrated circuit, comprising:

forming an array of memory cells on a substrate;

coupling a substrate voltage level controller circuit to the substrate for setting a substrate voltage bias level including:

coupling a series of diode connected transistors between a supply voltage source and the substrate; and

coupling at least one bypass transistor to a plurality of diode connected transistors in the series of diode connected transistors for electrically bypassing the plurality of diode connected transistors, wherein the at least one bypass transistor is adapted for selective actuation to both an on state and an off state by a user while setting a substrate voltage bias level.

39. (Previously Presented) The method of claim 38 wherein coupling at least one bypass transistor to a plurality of diode connected transistors includes coupling a plurality of

bypass transistors to a plurality of diode connected transistors in the series of diode connected transistors for electrically bypassing the plurality of diode connected transistors.

40. (Previously Presented) The method of claim 38 wherein coupling a plurality of bypass transistors to a plurality of diode connected transistors includes coupling a plurality of normally off bypass transistors to a plurality of diode connected transistors leaving the plurality of diode connected transistors unbypassed during normal operation and allowing the plurality of diode connected transistors to be selectively bypassed during testing operations.

41. (Previously Presented) The method of claim 38 wherein coupling a plurality of bypass transistors to a plurality of diode connected transistors includes coupling a plurality of normally on bypass transistors to a plurality of diode connected transistors leaving the plurality of diode connected transistors bypassed during normal operation and allowing the plurality of diode connected transistors to be selectively unbypassed during testing operations.

42. (Previously Presented) A method of forming an integrated circuit, comprising:

forming an array of memory cells on a substrate;

coupling a substrate voltage level controller circuit to the substrate for setting a substrate voltage bias level including:

coupling a series of diode connected transistors between a supply voltage source and the substrate; and

coupling a plurality of bypass transistors to a plurality of diode connected transistors in the series of diode connected transistors for electrically bypassing the plurality of diode connected transistors, wherein the at least one bypass transistor is adapted for selective actuation by a user to both an on state and an off state while setting a substrate voltage bias level.

43. (Previously Presented) The method of claim 42 wherein coupling a plurality of bypass transistors to a plurality of diode connected transistors includes coupling a plurality of normally off bypass transistors to a plurality of diode connected transistors leaving the plurality of diode connected transistors unbypassed during normal operation and allowing the plurality of diode connected transistors to be selectively bypassed during testing operations.

44. (Previously Presented) The method of claim 42 wherein coupling a plurality of bypass transistors to a plurality of diode connected transistors includes coupling a plurality of normally on bypass transistors to a plurality of diode connected transistors leaving the plurality of diode connected transistors bypassed during normal operation and allowing the plurality of diode connected transistors to be selectively unbypassed during testing operations.

45. (Previously Presented) A method of forming an integrated circuit, comprising:

forming an array of memory cells on a substrate;

coupling a substrate voltage level controller circuit to the substrate for setting a substrate voltage bias level including:

coupling a series of diodes between a supply voltage source and the substrate; and

coupling at least one bypass transistor to a plurality of diodes in the series of diodes for electrically bypassing a portion of the plurality of diodes, wherein the at least one bypass transistor is adapted for selective actuation to both an on state and an off state by a user while setting a substrate voltage bias level.

46. (Previously Presented) The method of claim 45 wherein coupling at least one bypass transistor to a plurality of diodes includes coupling at least one normally off bypass transistor to a plurality of diodes leaving the portion of the plurality of diodes unbypassed during normal operation and allowing the portion of the plurality of diodes to be selectively bypassed during testing operations.

47. (Previously Presented) The method of claim 45 wherein coupling at least one bypass transistor to a plurality of diodes includes coupling at least one normally on bypass

transistor to a plurality of diodes leaving the portion of the plurality of diodes bypassed during normal operation and allowing the portion of the plurality of diodes to be selectively unbypassed during testing operations.

48. (New) A method of forming an integrated circuit, comprising:

forming an array of memory cells on a substrate;

coupling a test circuit to the substrate, including:

coupling a series of resistive elements together in series to form a chain of elements having two terminals, the first terminal coupled to a supply voltage, and the second terminal coupled to the substrate; and

coupling a plurality of switches to respective resistive elements in the series of resistive elements for electrically bypassing the respective resistive elements, wherein the plurality of switches are adapted for selective actuation to both an on state and an off state by a user.

49. (New) The method of claim 48, wherein coupling a series of resistive elements together includes coupling a series of diodes together.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 373-6944 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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